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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2183

Examiner: Richard Ellis

Serial No.: 09/385,394 - 9093

Filed: August 30, 1999

I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on June 20, 2002 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, Washington D.C. 20231.

Applicant(s): John S. Yates, Jr., et al.

Title: COMPUTER FOR EXECUTING TWO DIFFERENT INSTRUCTION SETS

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COMMISSIONER FOR PATENTS
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RESPONSE TO OFFICE ACTION OF FEBRUARY 20, 2002

Kindly amend the application as follows.

07/01/2002 SSITHIB1 00000100 500675 09385394
02 FC:102 330.00 OP
03 FC:103 234.00 CH 450.00 OP

In the Title:

Kindly amend the title to -- COMPUTER WITH TWO EXECUTION MODES --.

In the claims:

Kindly rewrite the following claims as indicated:

1. (amended) A computer, comprising:

a processor pipeline designed to alternately execute instructions coded for first and second different computer architectures or coded to implement first and second different processing conventions;

a memory for storing instructions for execution by the processor pipeline, the memory being divided into pages for management by a virtual memory manager, a single address space of the memory having first and second pages;

a memory unit designed to fetch instructions from the memory for execution by the pipeline, and to fetch stored indicator elements associated with respective memory pages of the single address space from which the instructions are to be fetched, each indicator element